09/994,261

EGL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Albert MAN, et al.

Assignee: ATI, Inc.

Title: SYSTEM FOR TESTING DEVICES AND METHOD THEREOF

Patent No.: 6,961,885 B2 Issued: November 1, 2005

Atty. Docket No.: 1376-0100660

MS: Certificate of Correction Branch
COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT— PTO MISTAKE (37 C.F.R. § 1.322(a))

Dear Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), please issue a Certificate of Correction in the above-identified matter. The mistake(s) to be corrected was made by the Office.

1. Attached hereto, in duplicate, is Form PTO-1050, with at least one copy suitable for printing.
2. The exact page(s) and line number(s) where the error(s) is shown correctly in the application file:
   Response to Office Action mailed May 24, 2004, page number 5 of 12, Claim 12 (a copy of which is attached).
3. Please send the Certificate to:

J. Gustav Larson
TOLER, LARSON & ABEL, LLP
5000 PLAZA ON THE LAKE, SUITE 265
AUSTIN, TX 78746

Respectfully submitted,

1-5-06
Date

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PTO/SB/44 (05-03)
Approved for use through 01/31/2004. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,961,8885 B2

DATED : November 1, 2005

INVENTOR(S) : Albert Man, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, line 24: Please change "system: as" to "system as"

(Also Form PTO-1050)

MAILING ADDRESS OF SENDER:
TOLER, LARSON & ABEL, LLP
5000 Plaza On The Lake, Suite 265
Austin, TX 78746

PATENT NO. 6,961,885 B2 **Error! Reference source not found.**

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Albert Man et al.		
Title:	SYSTEM FOR TESTING DEVICES AND METHOD THEREOF		
App. No.:	09/994,261	Filed:	11/26/2001
Examiner:	David Ton	Group Art Unit:	2133
Customer No.:	34456	Confirmation No.:	8626
Atty. Dkt. No.:	1376-0100660		

Mail Stop Non-Fee Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed February 24, 2004, please amend the above-identified application as follows:

CERTIFICATE OF TRANSMISSION/MAILING
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to the Commissioner for Patents on 5-24-04.

Katrina Prati
Typed or Printed Name

Katrina Prati
Signature

IN THE SPECIFICATION:

Please amend the title of invention as follows:

SYSTEM AND METHOD FOR TESTING VIDEO DEVICES USING A TEST FIXTURE~~AND METHOD THEREOF~~

IN THE CLAIMS:

Please amend claims 1-5, 7-9 and 11 as indicated in the following:

Claims Listing:

1. (Currently Amended) A method of production testing a video device comprising ~~the steps of~~:

coupling~~mounting~~ a device to~~on~~ a test fixture, wherein the test fixture is coupled to a general-purpose computer;

testing the device using one or more scan techniques, wherein testing the device includes:

serially providing a first test vector to the device via the test fixture;

clocking the device to assert the first test vector within the device;

serially providing a second test vector to the device via the test fixture;

receiving results from the first test vector concurrently with the step of providing the second test vector; and

comparing the results with expected results.

2. (Currently Amended) The method as in Claim 1, wherein ~~the step of~~ testing the device using the one or more scan-test techniques includes ~~the step of~~ determining, after ~~the step of~~ comparing the results, if the device has passed a scan-test, wherein the device has passed the scan-test when the results are equivalent to the expected results and the device has failed the scan-test when the results are different from the expected results.

3. (Currently Amended) The method as in Claim 2, wherein ~~the step of~~ testing the device using the one or more scan-test techniques further includes ~~the step of~~ placing the device in a good bin when the device has passed the scan-test.

4. (Currently Amended) The method as in Claim 3, wherein the device is taken from the good bin for ~~performing the step of~~ testing the device using an at speed test.

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5. (Currently Amended) The method as in Claim 2, wherein ~~the step of~~ testing the device using the one or more scan-test techniques further includes ~~the step of~~ placing the device in a bad bin when the device has failed the scan-test.

6. (Original) The method as in Claim 1, wherein the device is a video processing device.

7. (Currently Amended) The method as in Claim 1, wherein ~~the step of~~ serially providing the first test vector to the device includes providing multiple chains of serial test vector values to separate sets of components of the device for concurrently testing the sets of components.

8. (Currently Amended) The method as in Claim 1, further including ~~the steps of~~:
selecting one of an at speed test mode and a scan-test mode; and
testing the device using an at-speed test when the at speed test mode is selected.

9. (Currently Amended) The method as in Claim 8, wherein the device is tested using the one or more scan techniques before the device is tested using the at speed test.

10. (Original) The method as in Claim 1, wherein the general-purpose computer includes one of a peripheral component interconnect port, an accelerated graphics port, a serial port, a JTAG port, or a parallel port for interfacing with the test fixture.

11. (Currently Amended) A system comprising:
a general purpose computer having:
a data processor having an input/output buffer;
memory having an input/output buffer coupled to the input/output buffer of the data processor, said memory including a set of instructions to provide a scan-test pattern for testing a device;
a communications port having an input/output buffer coupled to the input/output buffer of the data processor;
a test fixture having:
a communications interface coupled to the communications port, the communications port to receive said scan-test pattern;

a scan-chain selector for selecting a particular scan-chain of a plurality of scan chains in said device for testing;

a control module to:

generate signals to set said device in a scan-test mode;

provide said signals to a device socket;

load said scan-test pattern, through said device socket, into said particular scan-chain of said device;

provide a clock signal to said device socket, wherein said clock signal is to latch output results from said particular scan-chain;

said device socket for interfacing with said device, said device socket to:

provide said signals and said scan-test pattern from said control module to said particular scan-chain of said device and;

receive said output results.

12. (Original) The system as in Claim 11, wherein said communications port includes a JTAG port.

13. (Original) The system as in Claim 11, wherein said communications port includes an accelerated graphics port.

14. (Original) The system as in Claim 11, wherein said scan chain selector is configured by a user to select said particular scan chain.

15. (Original) The system as in Claim 11, wherein said scan-chain selector is configured by said set of instructions, through said control module.

16. (Original) The system as in Claim 11, wherein said device includes a graphics processor.

17. (Original) A test fixture comprising:

a bus interface for receiving test signals;

a test mode selector coupled to the bus interface, said test mode selector to route said test signals from said bus interface to one of an at-speed operating path and a scan-test path;

a scan-test control module coupled to said scan-test path of said test mode selector, said scan-test control module to:

engage a scan-test mode in a device;

selecting a particular scan-chain of a plurality of scan-chains associated with said device;

providing a scan pattern to a test socket, wherein said scan pattern is loaded into said scan-chain;

receiving results from said device, wherein results are related to said scan pattern;

a test socket having:

a first input/output buffer coupled to said at-speed operating path of said test mode selector;

a second input/output buffer coupled to said scan-test path of said test mode selector; and

a third input/output buffer coupled buffer coupled to said device.

18. (Original) The test fixture as in Claim 17, wherein said bus interface includes an accelerated graphics port interface.

19. (Original) The test fixture as in Claim 17, wherein said bus interface is coupled to a bus port of an information handling system.

20. (Original) The test fixture as in Claim 17, wherein the test mode selector is configured through said test signals to select from one of the at-speed operating path and the scan-test path.

21. (Original) The test fixture as in Claim 17, wherein the at-speed operating path is used to provide test signals associated with at-speed tests.

22. (Original) The test fixture as in Claim 17, wherein said device includes a graphics processor.

REMARKS

The Office Action dated February 23, 2004 has been received and carefully considered. Claims 1-5, 7-9 and 11 have been amended. No new matter is introduced by the amendments to these claims. Reconsideration of the outstanding rejections in the present application therefore is respectfully requested based on the following remarks.

Allowability of Claims 17-22

The Applicants note with appreciation the Examiner's indication at page 9 of the Office Action that claims 17-22 are allowable.

Objection to the Title of the Invention

At page 2 of the Office Action, the title of the invention was objected to as not clearly indicative of the invention to which the claims are directed. The Applicants have amended the title of the invention to more clearly indicate the claimed invention. The Applicants therefore respectfully request withdrawal of this objection.

Obviousness Rejection of Claims 1-10

At page 2 of the Office Action, claims 1, 6 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoang (U.S. Patent No. 6,357,026) in view of Zasio (U.S. Patent No. 4,504,783) and further in view of Buckley (U.S. Patent No. 5,969,756). At page 5 of the Office Action, claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoang in view of Zasio and further in view of Buckley and Blasco (U.S. Patent No. 6,691,270). At pages 5-6 of the Office Action, claims 2-5, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hoang in view of Zasio and further in view of Buckley and Yousuf (U.S. Patent No. 6,128,757). These rejections are respectfully traversed.

Claim 1, from which claims 2-10 depend, has been amended to recite a method of production testing a video device, where the method comprises, in part, the limitations of coupling a device to a test fixture, serially providing a first test vector to the device via the test fixture, clocking the device to assert the first test vector within the device, and serially providing

a second test vector to the device via the test fixture. The Examiner asserts that the combination of the teachings of Hoang, Zasio and Buckley discloses at least these limitations. However, it is respectfully submitted that, contrary to the Examiner's assertions, this proposed combination is contrary to the teachings of Hoang and therefore is improper, and even if so combined, these references fail to disclose each and every limitation of claim 1.

The Examiner proposes that one of ordinary skill in the art would be motivated to combine the teachings of Hoang and Zasio because "[such a combination] would use Zasio's test system for testing, diagnostic and evaluations [sic] Hoang's ASIC." Office Action, p. 3. However, it is submitted that Hoang teaches a method for testing interconnects by "[generating] binary progressive scan patterns for the output registers of one ASIC that are scanned and captured at the input registers of another ASIC. The test results are stored in a multiple input shift register (MISR) where they can be accessed for examination and diagnostic evaluations." Hoang, col. 1, lines 48-53. Thus, Hoang teaches a technique whereby the interconnects between the two ASICs may be tested by outputting binary scan patterns from an output of one of the ASICs to the other ASIC. The advantage of this arrangement, as taught by Hoang, is that "because the self-test is autonomous within each ASIC, *no further external components are added to the circuitry to implement a test.*" Hoang, col. 1, lines 64-67 (emphasis added). Thus, modifying the autonomous two-ASIC interconnect testing technique taught by Hoang by adding the tester fixture taught by Zasio negates the autonomous purpose of the interconnect testing technique taught by Hoang as it adds external components to the circuitry (a situation which the disclosure of Hoang expressly seeks to avoid).

Moreover, as noted above, claim 1 recites, in part, the limitations of serially providing first and second test vectors to the device *via the test fixture.* Hoang, however, teaches that the progressive binary patterns (which the Examiner appears to equate to test vectors) are generated internally at ASIC 12 before being provided to ASIC 14 to test the interconnect between the ASIC 12 and the ASIC 14 (see, e.g., Hoang, col. 2, lines 46-49 and col.3, lines 39-67). As the progressive binary patterns are generated internally, the system of Hoang has no need for progressive binary patterns/test vectors to be supplied from an external component such as the test fixture of Zasio, and to do so would destroy the functionality of Hoang as such a test would

no longer be "autonomous within each ASIC" and would introduce "further external components" to implement the test.

Even if so combined, the Applicants respectfully submit that the teachings of Hoang and Zasio fail to disclose or suggest each and every limitation recited by claim 1. As noted above, claim 1 recites, in part, the limitations of clocking the device to assert the first test vector within the device. With respect to these limitations, the Examiner asserts that the phrase "shifting the first binary pattern into an output register" from claim 1 (col. 4, line 15) of Hoang discloses clocking the device to assert the first test vector within the device. The Applicants respectfully submit that this phrase from Hoang merely discloses placement of the first binary pattern on an output register and has no relation to any type of clocking, much less clocking the device so as to assert a test vector within the device as recited in claim 1.

Accordingly, because the combination of Hoang and Zasio is improper for at least the reasons provided above, the combinations of Hoang, Zasio, Buckley, Blasco and Yousuf proposed by the Examiner are improper for at least the same reasons. Moreover, the Applicants respectfully submit that the Examiner has failed to establish how these references disclose or even suggest, alone or in combination, at least the limitations of clocking a device to assert the first test vector within the device as recited in claim 1.

In view of the foregoing, it is respectfully submitted that the cited references fail to disclose or even suggest each and every limitation of claim 1 and therefore fail to disclose or suggest each and every limitation of claims 2-10 at least by virtue of their dependency on claim 1. Moreover, these claims recite additional features that are not disclosed or even suggested by the cited references taken either alone or in combination. Accordingly, the Applicants respectfully submit that the obviousness rejections of claims 1-10 are improper at this time and withdrawal of these rejections therefore is respectfully requested.

Obviousness Rejection of Claims 11-16

At page 7 of the Office Action, claims 11-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Blasco in view of Pierre (U.S. Patent No. 6,539,510). This rejection is respectfully traversed.

Claim 11, from which claims 12-16 depend, recites, in part, the limitations of a system comprising a test fixture having a scan-chain selector for selecting a particular scan-chain of a plurality of scan chains in a device for testing and having a control module to load a scan test pattern, through a device socket, into a particular scan chain of the device and to provide a clock signal to the device socket, wherein the clock signal is to latch output results from the particular scan-chain. The Examiner asserts that the proposed combination of the teachings of Blasco and Pierre discloses at least these limitations. However, it is respectfully submitted that the Examiner has not demonstrated how and where Blasco discloses the particular limitations associated with each of the communications interface, the scan chain selector, and the control module that are recited in claim 11. With respect to these limitations, the Examiner merely provides that Blasco teaches "[a] test fixture [integrated circuit 120 of Fig. 1] having a communications interface [TAP of Fig. 1], a scan chain selector [Fig. 2], a control module [TAP controller 18 of Fig. 1]." Office Action, p. 8. Should the Examiner continue to assert this rejection in view of the remarks below, Applicants respectfully request that the Examiner provide a more detailed explanation as to how Blasco purportedly teaches these limitations.

With respect to the rejection of Claim 11, the Examiner asserts that the integrated circuit 120 of Blasco is analogous to the test fixture recited in claim 11. However, the Applicants respectfully submit that this analogy is inconsistent with the subject matter of claim 11 and the teachings of the present application. Claim 11 recites the limitations of a system having a test fixture and a device socket for interfacing with a device, where the device socket provides signals and the scan-test pattern from a control module of the test fixture to the device and receives output results. Thus, it is understood from the context of claim 11 that the test fixture is separate from, or not part of, the device being tested. In contrast, Blasco teaches an integrated circuit having both the circuitry to be tested and the debugging logic 130 (including the TAP controller 18), and therefore fails to disclose a test fixture separate from the device being tested. Moreover, the integrated circuit of Blasco has no need for a device socket to couple an external test fixture to the device because the device and the debugging logic (i.e., the test fixture) are integrated. Consequently, there is no motivation for one of ordinary skill in the art to modify the teachings of Blasco so as to include an interface board having a socket as allegedly taught by Pierre because such a modification is contrary to the functioning of the integrated circuit disclosed by Blasco. Accordingly, it is respectfully submitted that the obviousness rejection of

claims 11-16 is improper at this time and withdrawal of this rejection therefore is respectfully requested.

Conclusion

In view of the foregoing, the Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants do not believe that any additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

May 24, 2004
Date

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On Behalf Of
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